Fig.1

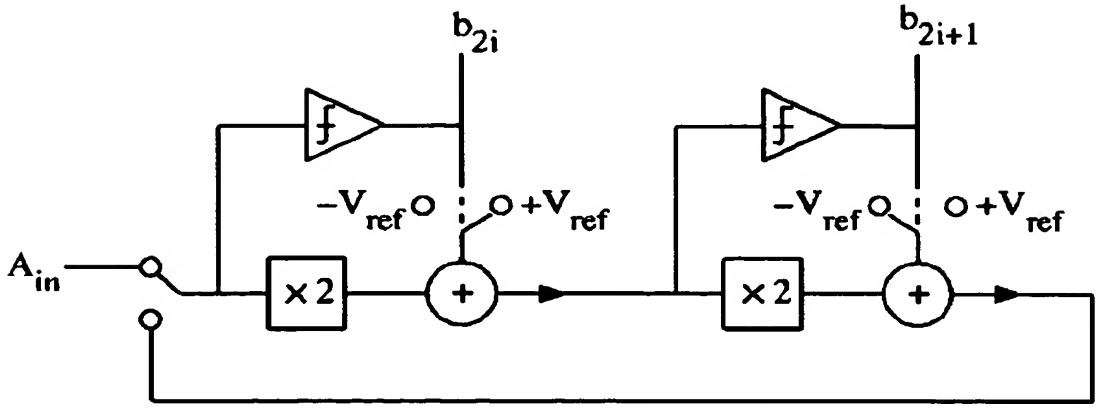

b_{2i}
b_{2i+1}
$-V_{ref}$
$+V_{ref}$
$-V_{ref}$
$+V_{ref}$
A_{in}
×2
+
×2
+

Fig.2

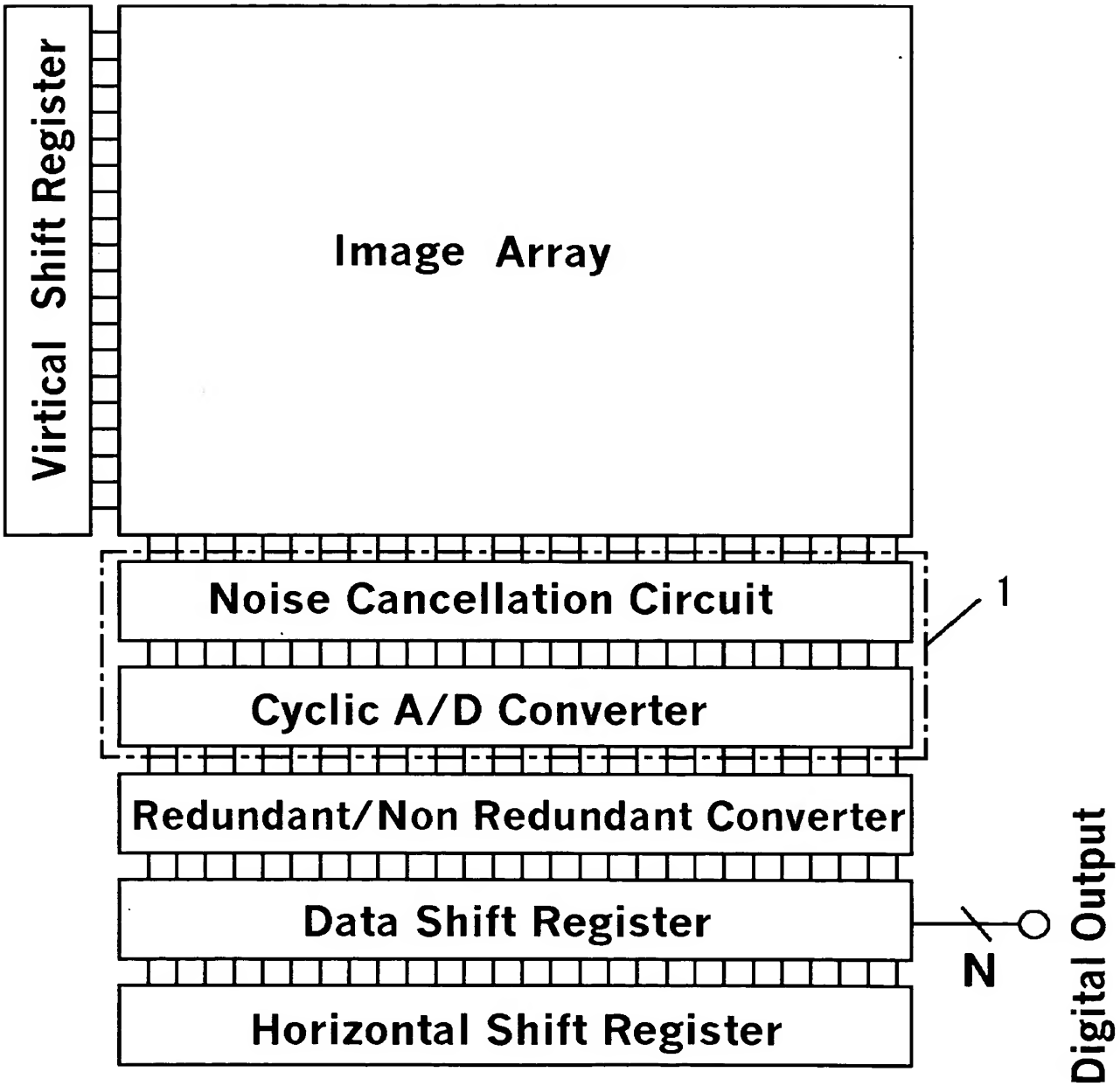

Virtical Shift Register
Image Array
Noise Cancellation Circuit
Cyclic A/D Converter
1
Redundant/Non Redundant Converter
Data Shift Register
N
Digital Output
Horizontal Shift Register

Fig.3

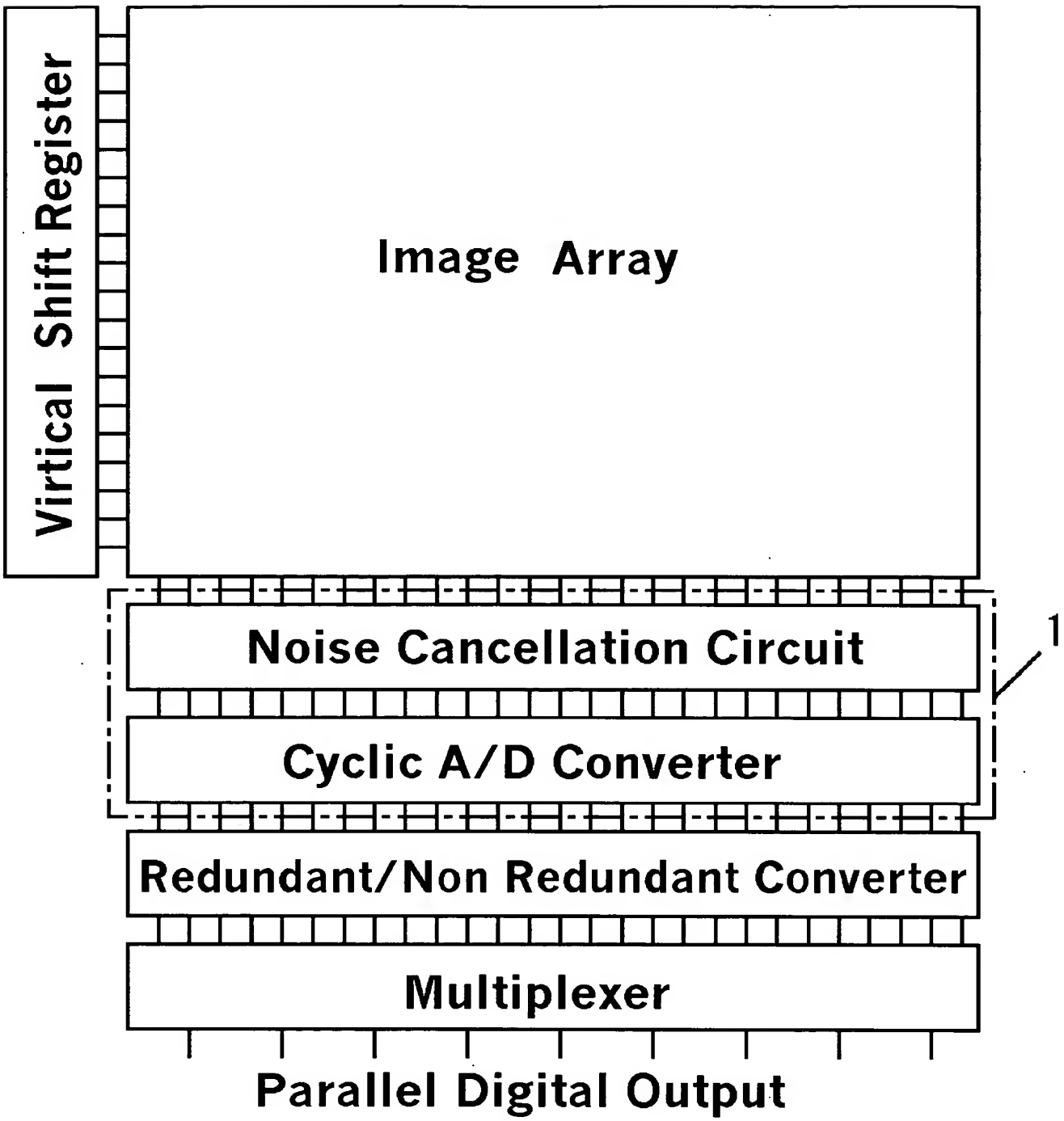

Virtical Shift Register
Image Array
Noise Cancellation Circuit
Cyclic A/D Converter
Redundant/Non Redundant Converter
Multiplexer
Parallel Digital Output
1

Fig.4

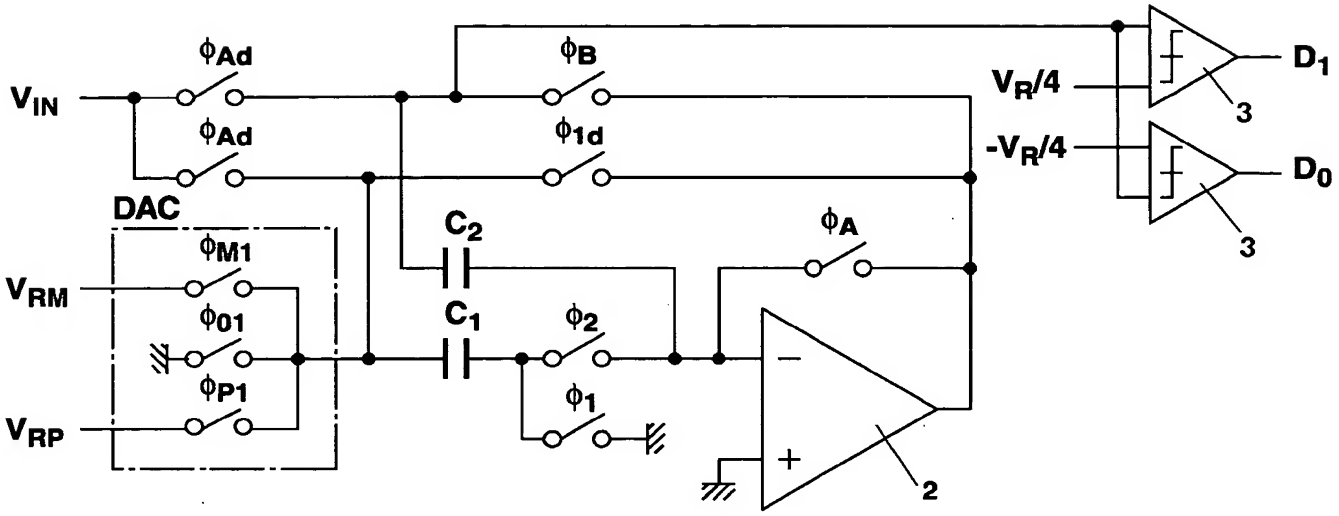

ϕ_{Ad}
ϕ_B
V_{IN}
ϕ_{Ad}
ϕ_{1d}
DAC
ϕ_{M1}
C_2
ϕ_A
V_{RM}
ϕ_{01}
C_1
ϕ_2
ϕ_{P1}
ϕ_1
V_{RP}
$V_R/4$
$-V_R/4$
D_1
D_0
3
3
2

Fig.5

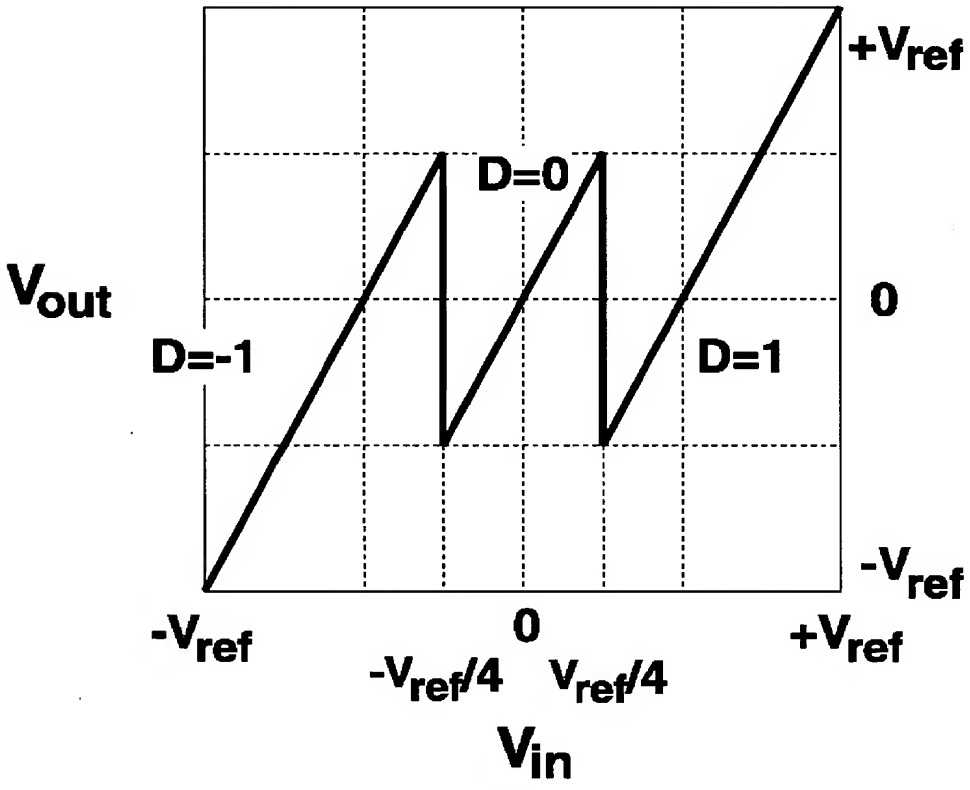

$+V_{ref}$
D=0
V_{out}
0
D=-1
D=1
$-V_{ref}$
$-V_{ref}$
0
$+V_{ref}$
$-V_{ref}/4$
$V_{ref}/4$
V_{in}

Fig.6

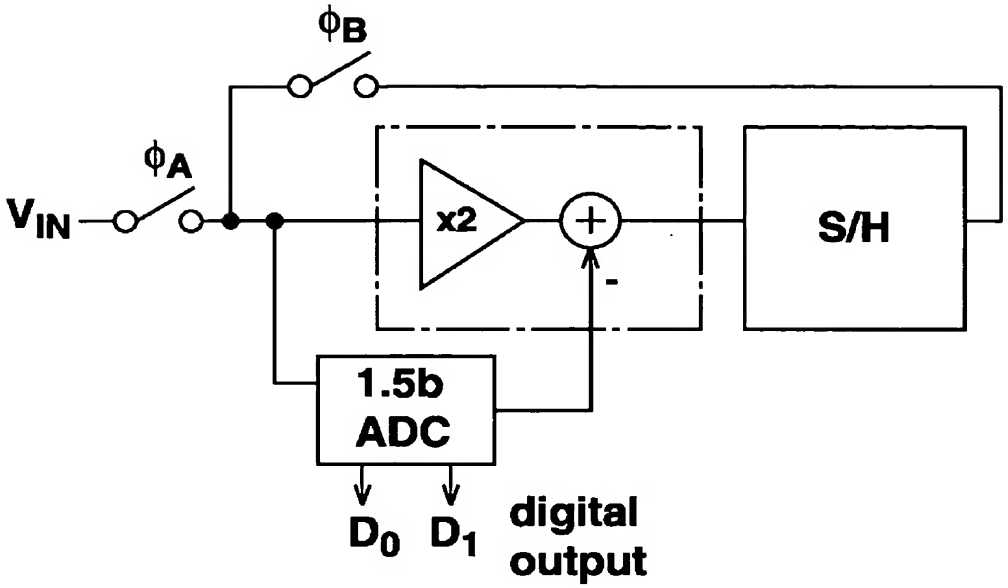

ϕB
ϕA
VIN
x2
+
-
S/H
1.5b
ADC
D0
D1
digital
output

Fig.7

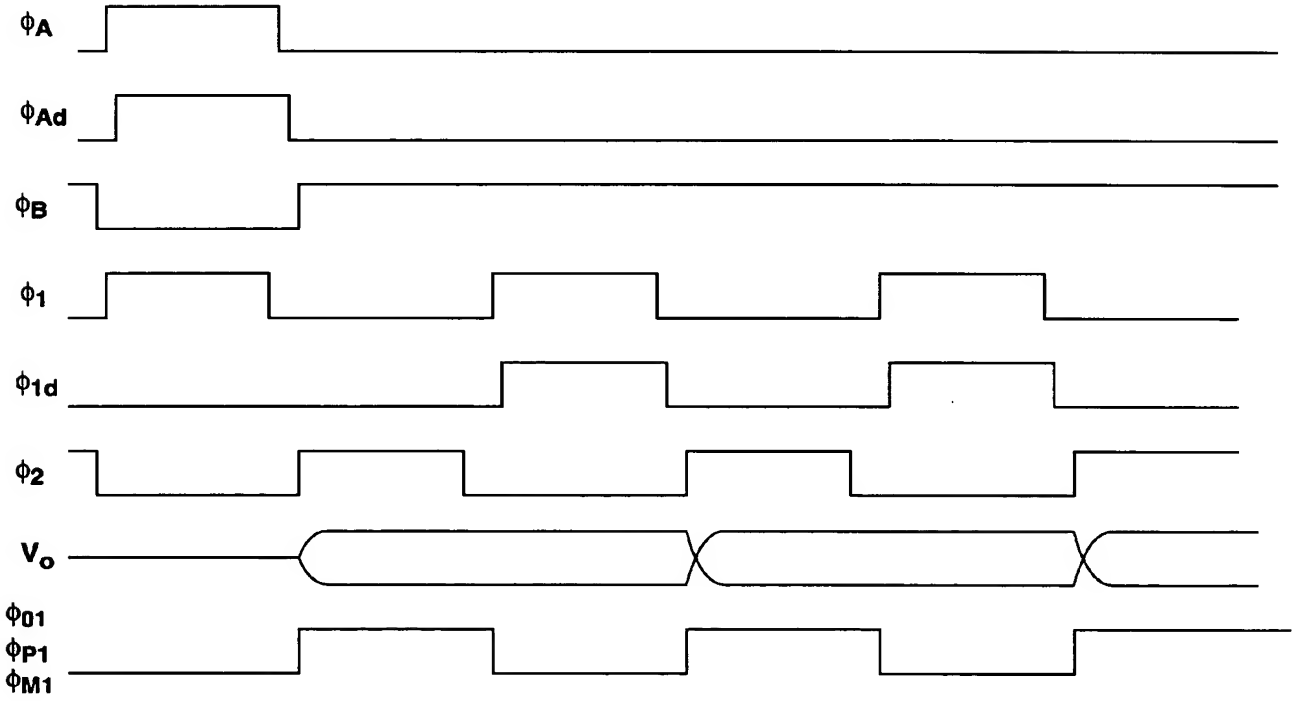

ϕA
ϕAd
ϕB
ϕ1
ϕ1d
ϕ2
Vo
ϕ01
ϕP1
ϕM1

Fig.8

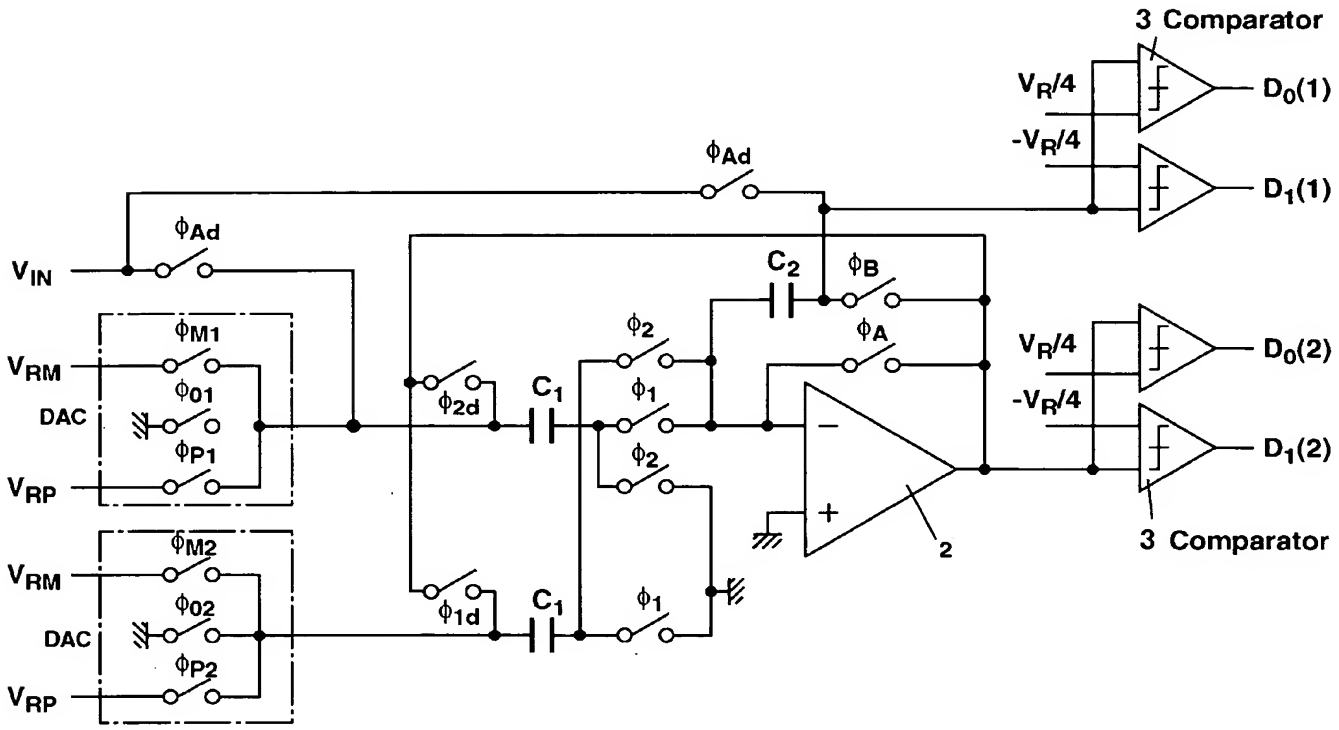

3 Comparator
$V_R/4$
$-V_R/4$
$D_0(1)$
$D_1(1)$
ϕ_{Ad}
V_{IN}
C_2
ϕ_B
ϕ_{M1}
V_{RM}
ϕ_{01}
DAC
ϕ_{P1}
V_{RP}
ϕ_{2d}
C_1
ϕ_2
ϕ_1
ϕ_A
$V_R/4$
$-V_R/4$
$D_0(2)$
$D_1(2)$
ϕ_{M2}
V_{RM}
ϕ_{02}
DAC
ϕ_{P2}
V_{RP}
ϕ_{1d}
C_1
ϕ_1
2
3 Comparator

Fig.9

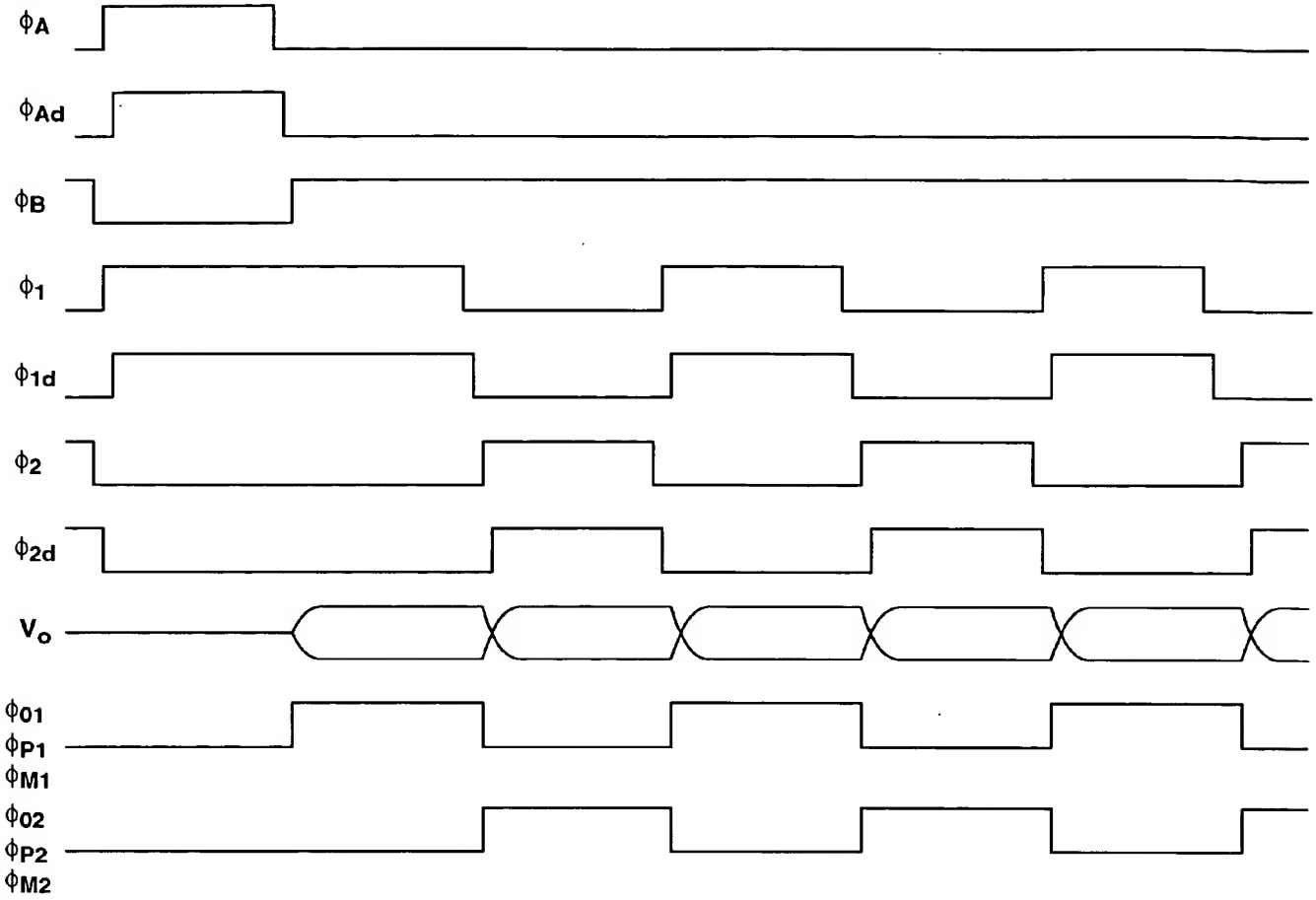

φA
φAd
φB
φ1
φ1d
φ2
φ2d
Vo
φ01
φP1
φM1
φ02
φP2
φM2

Fig.10

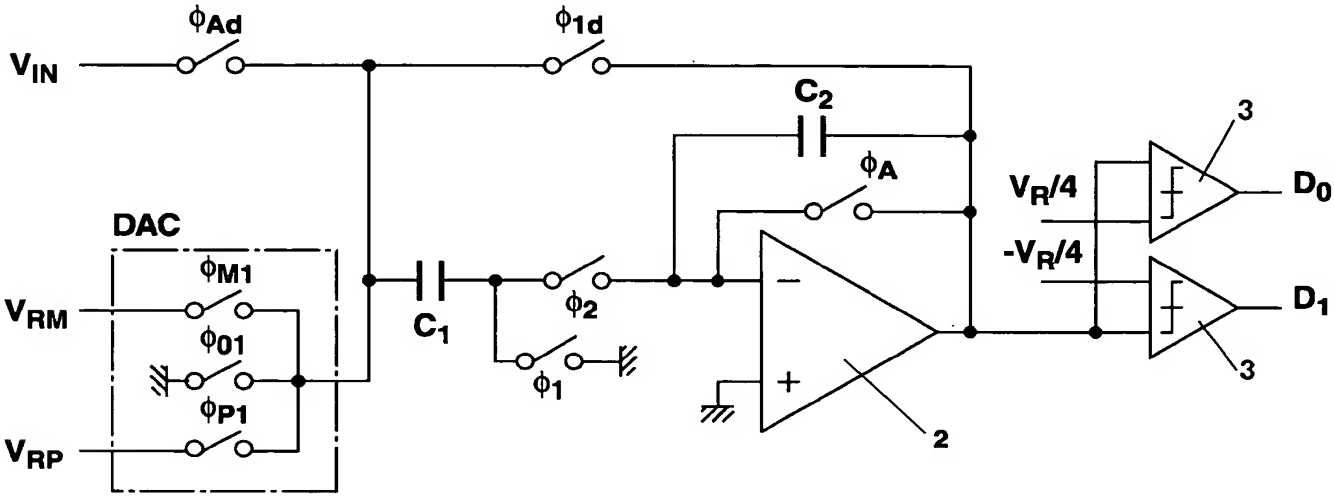

φAd
φ1d
VIN
C2
φA
VR/4
-VR/4
D0
D1
3
3
DAC
φM1
φ01
φP1
VRM
VRP
C1
φ2
φ1
2

Fig.11

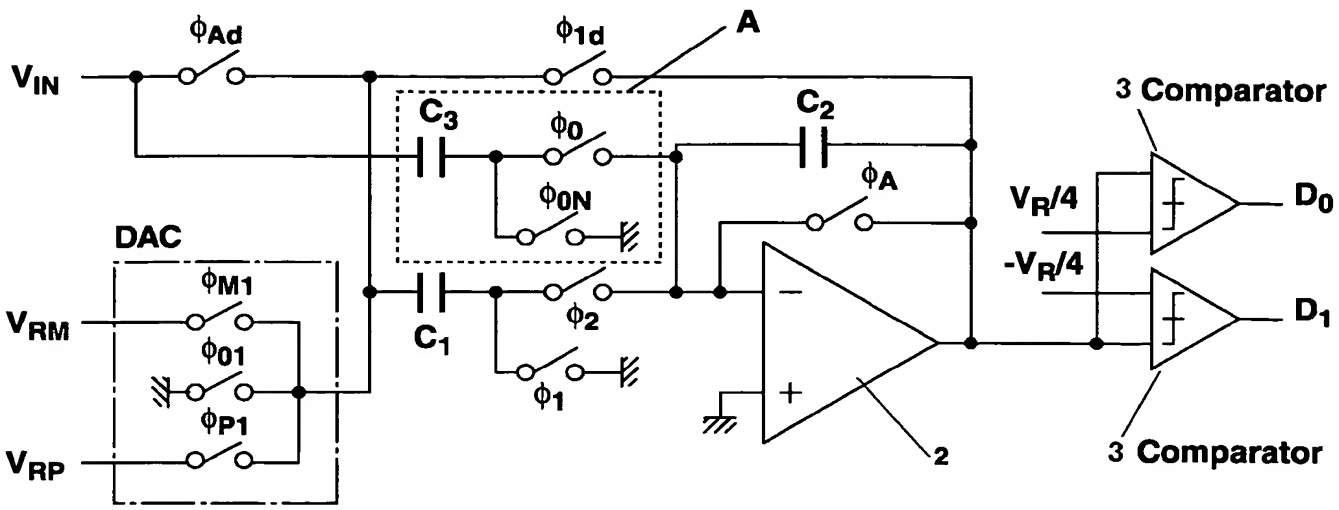

ϕ_{Ad}
ϕ_{1d}
A
V_{IN}
C_3
ϕ_0
ϕ_{0N}
C_2
ϕ_A
3 Comparator
$V_R/4$
D_0
DAC
ϕ_{M1}
V_{RM}
ϕ_{01}
C_1
ϕ_2
$-V_R/4$
D_1
ϕ_{P1}
ϕ_1
V_{RP}
2
3 Comparator

Fig.12

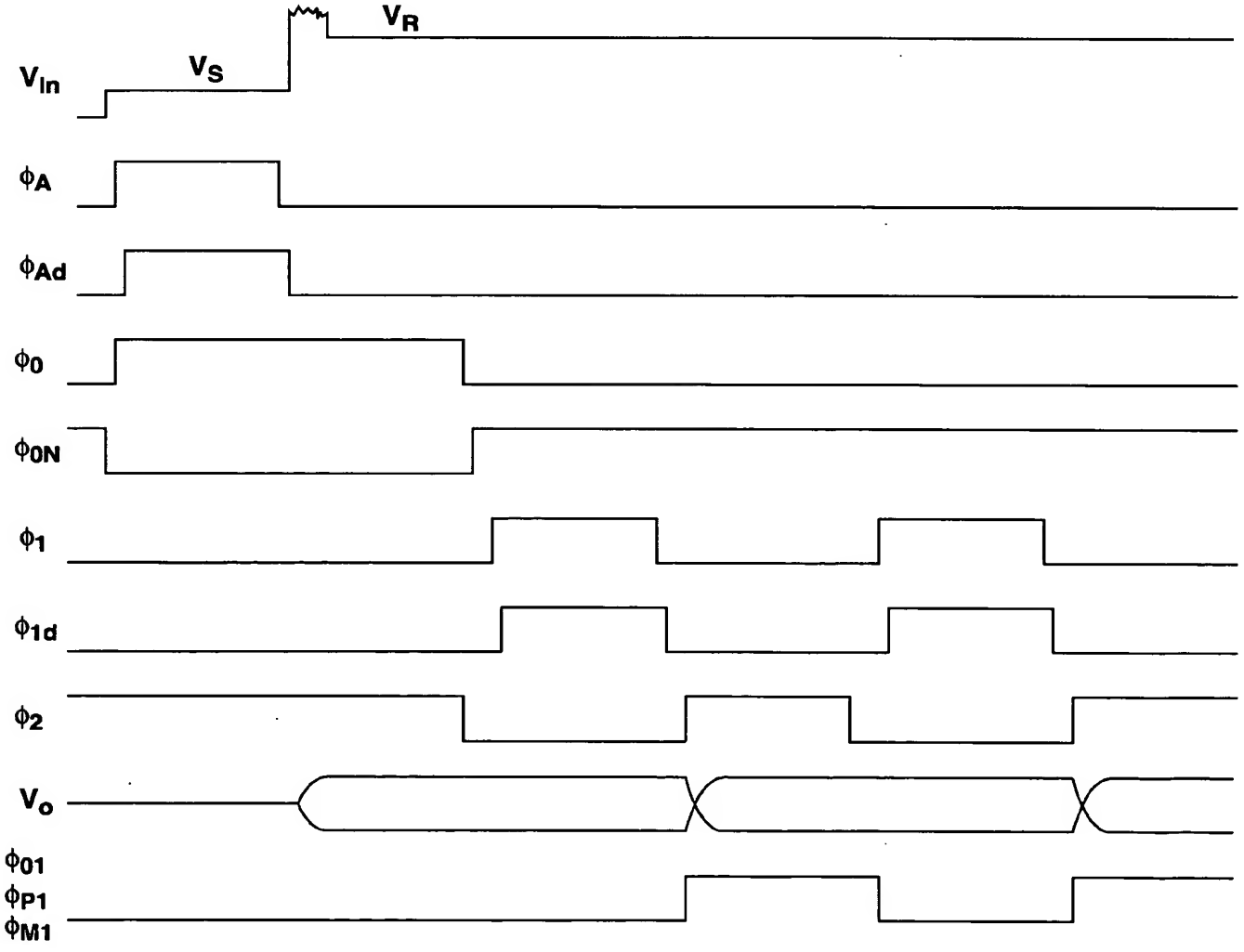

V_R
V_{In}
V_S
ϕ_A
ϕ_{Ad}
ϕ_0
ϕ_{0N}
ϕ_1
ϕ_{1d}
ϕ_2
V_o
ϕ_{01}
ϕ_{P1}
ϕ_{M1}

Fig.13

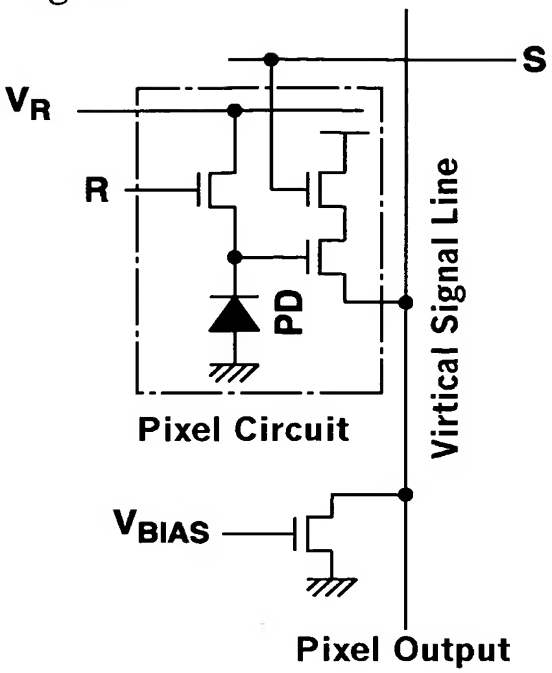

S
V_R
R
PD
Virtical Signal Line
Pixel Circuit
V_{BIAS}
Pixel Output

Fig.14

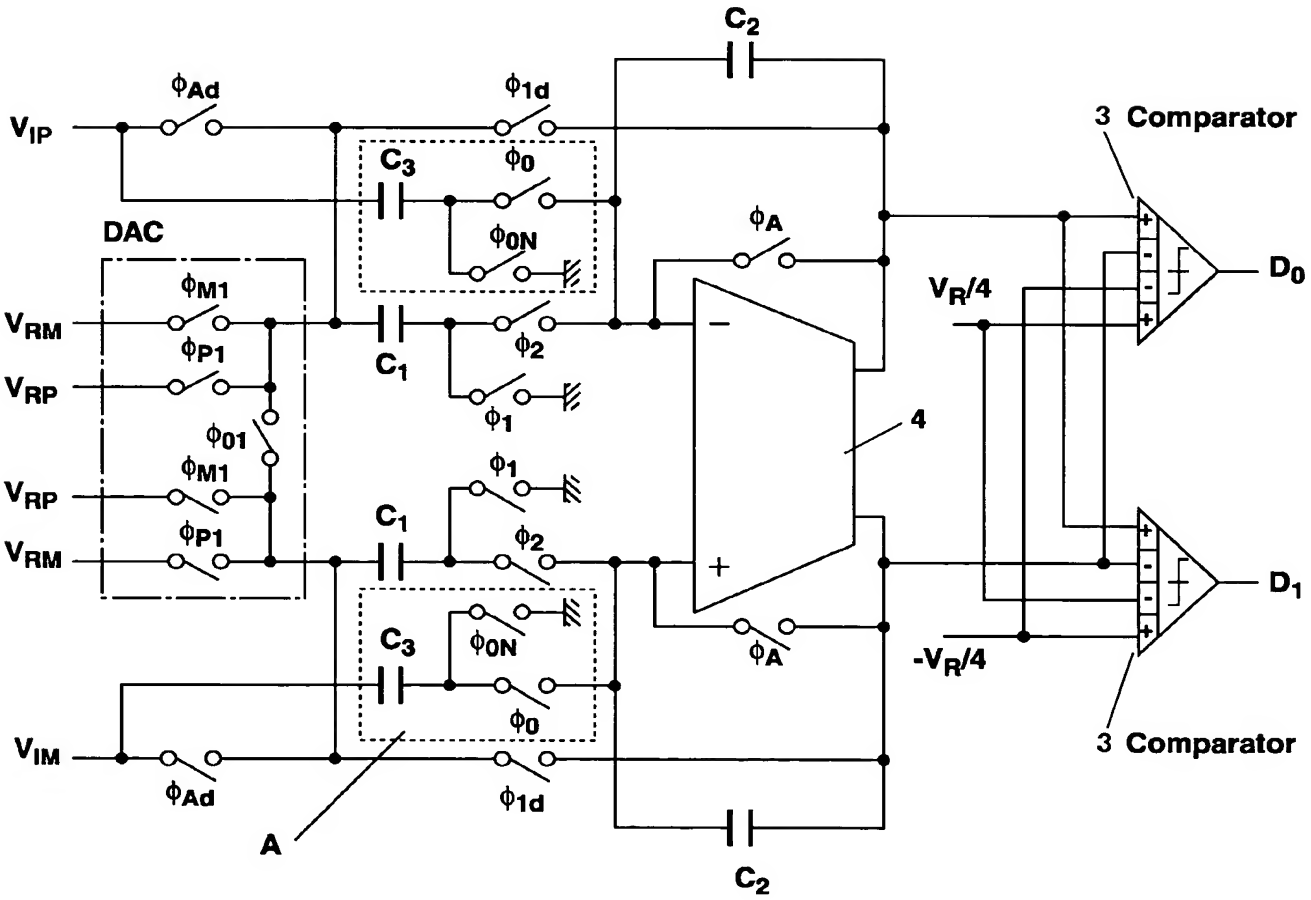

C_2
ϕ_{Ad}
ϕ_{1d}
V_{IP}
3 Comparator
C_3
ϕ_0
ϕ_{0N}
ϕ_A
DAC
ϕ_{M1}
V_{RM}
ϕ_{P1}
V_{RP}
C_1
ϕ_2
ϕ_1
$V_R/4$
D_0
ϕ_{01}
4
V_{RP}
ϕ_{M1}
V_{RM}
ϕ_{P1}
D_1
$-V_R/4$
V_{IM}
A
3 Comparator
C_2

Fig.15

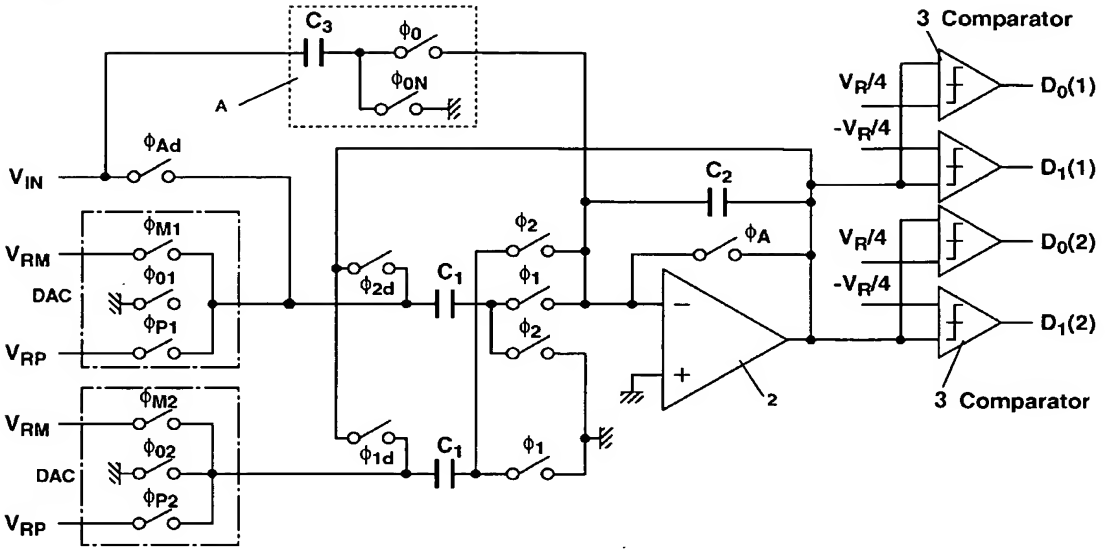

C3
φ0
φ0N
A
φAd
VIN
φM1
VRM
φ01
DAC
φP1
VRP
φM2
VRM
φ02
DAC
φP2
VRP
φ2d
C1
φ2
φ1
φ2
φA
C2
φ1d
C1
φ1
2
3 Comparator
VR/4
-VR/4
D0(1)
D1(1)
VR/4
-VR/4
D0(2)
D1(2)
3 Comparator

Fig.16

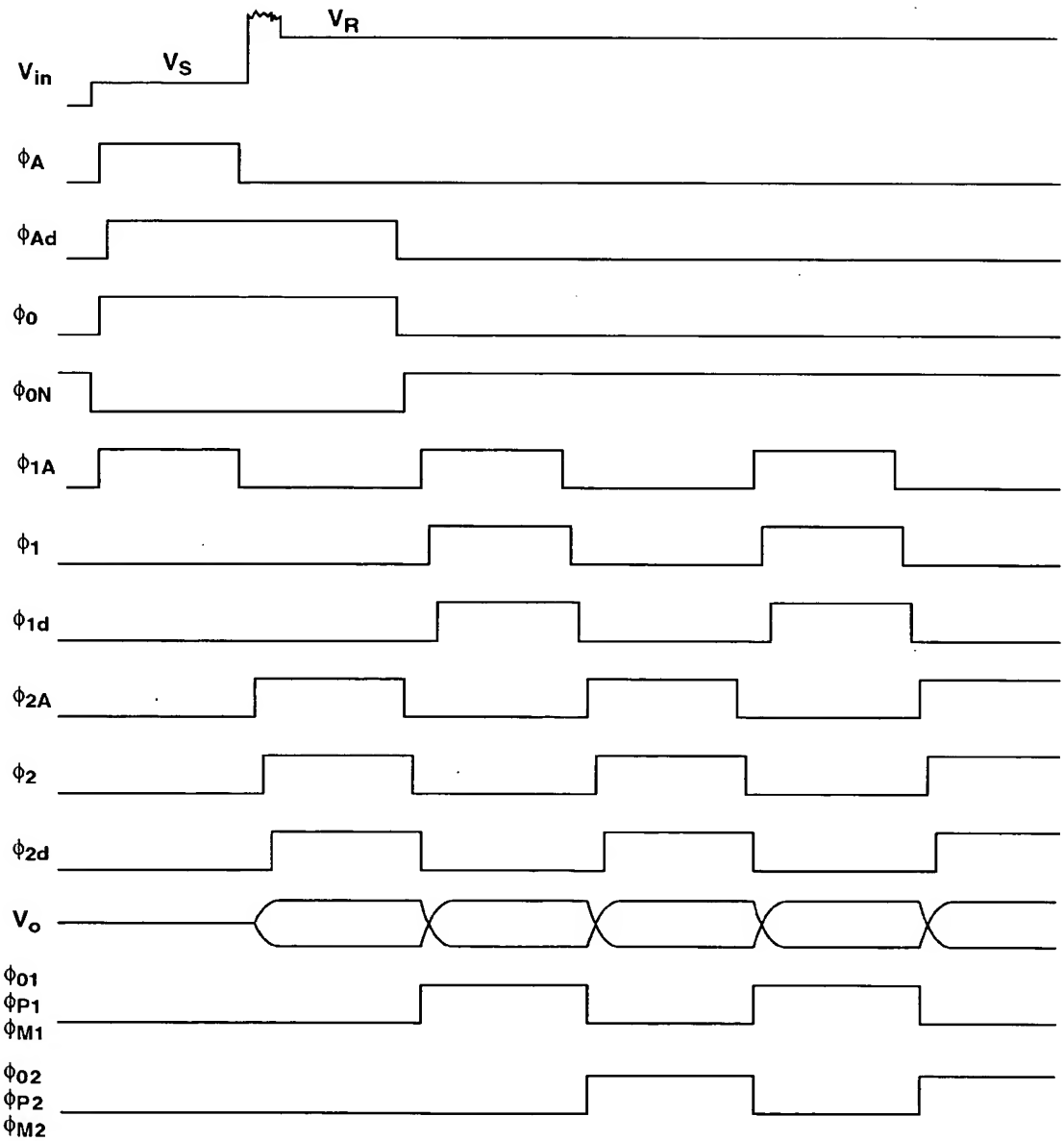

VR
Vin
VS
φA
φAd
φ0
φ0N
φ1A
φ1
φ1d
φ2A
φ2
φ2d
Vo
φ01
φP1
φM1
φ02
φP2
φM2

Fig.17

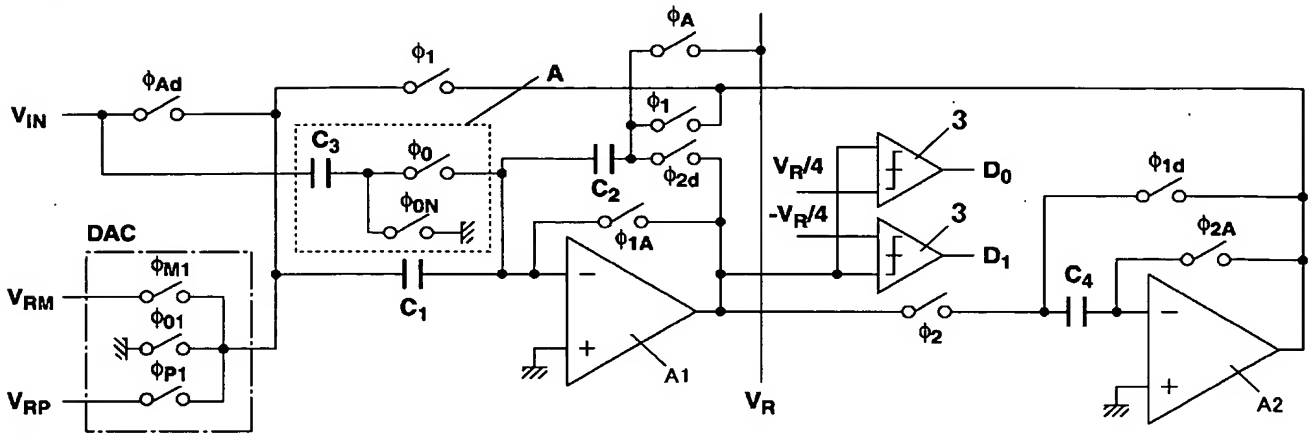

ϕ_A
ϕ_1
ϕ_{Ad}
A
V_{IN}
C_3
ϕ_0
ϕ_{0N}
C_2
ϕ_{2d}
ϕ_1
$V_R/4$
$-V_R/4$
3
3
D_0
D_1
ϕ_{1d}
ϕ_{2A}
DAC
ϕ_{M1}
V_{RM}
ϕ_{01}
ϕ_{P1}
V_{RP}
C_1
ϕ_{1A}
A1
V_R
ϕ_2
C_4
A2

Fig.18

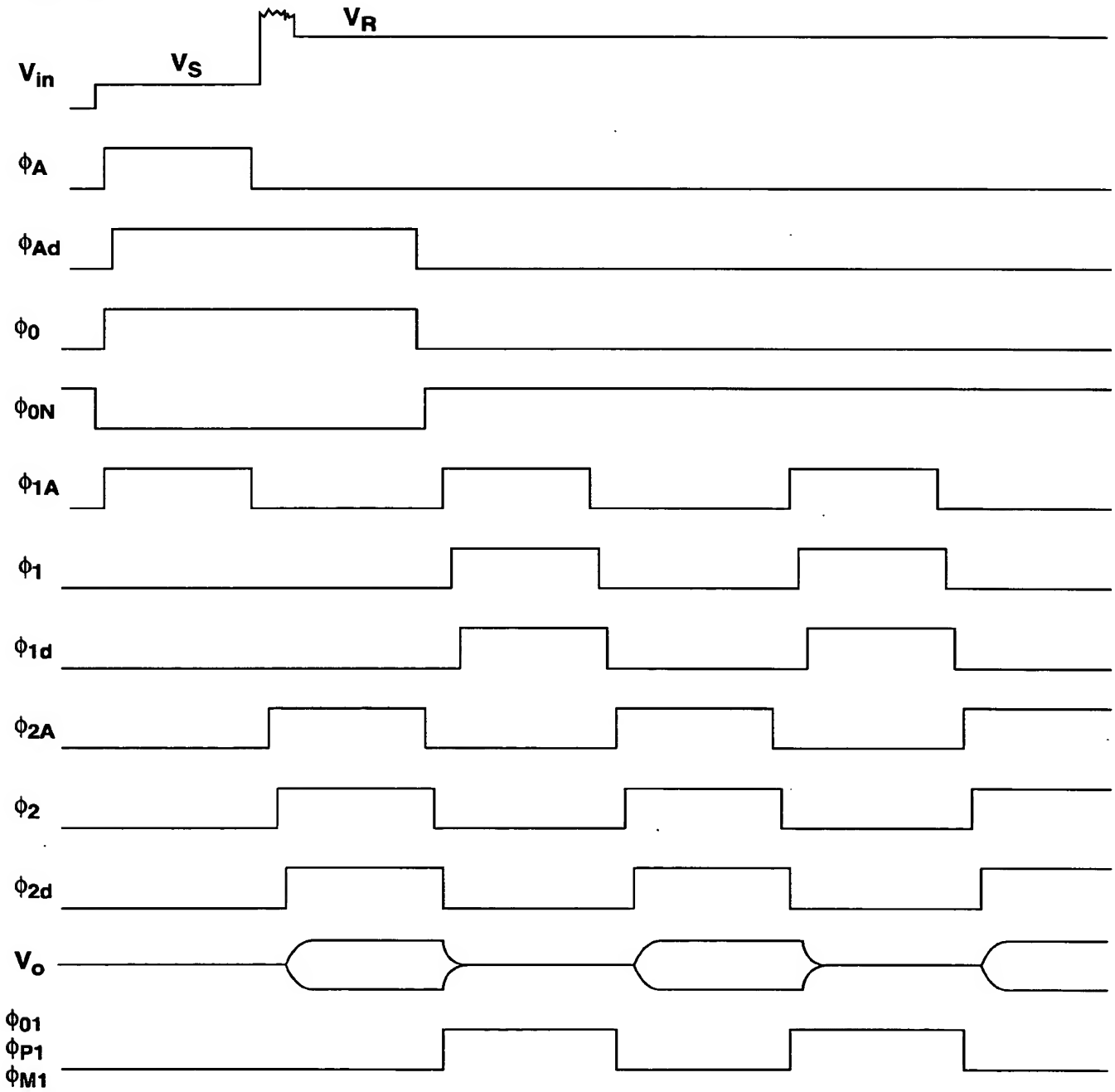
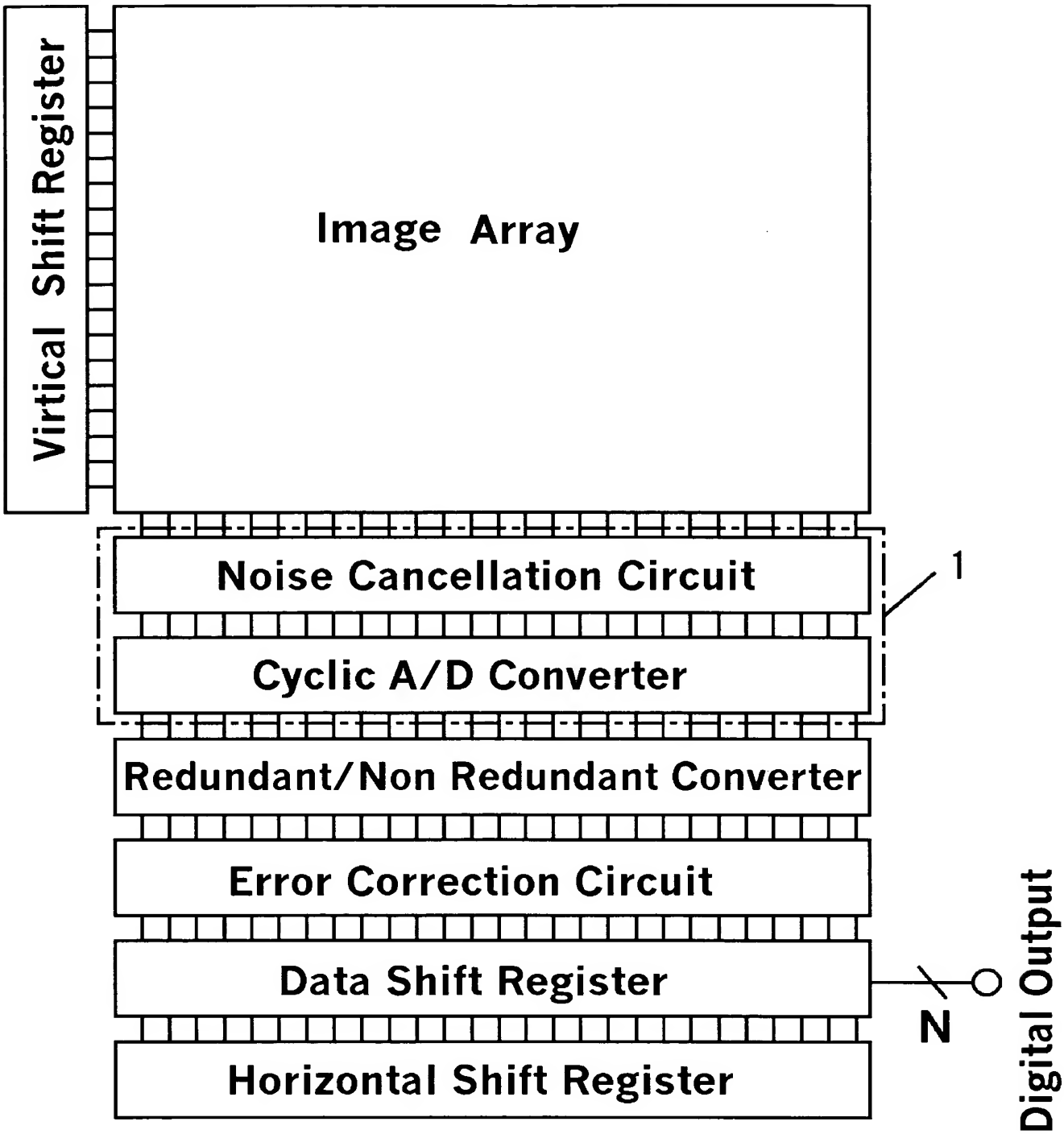

V_R
V_{in}
V_S
ϕ_A
ϕ_{Ad}
ϕ_0
ϕ_{0N}
ϕ_{1A}
ϕ_1
ϕ_{1d}
ϕ_{2A}
ϕ_2
ϕ_{2d}
V_o
ϕ_{01}
ϕ_{P1}
ϕ_{M1}

Fig.19


Virtical Shift Register
Image Array
Noise Cancellation Circuit
Cyclic A/D Converter
1
Redundant/Non Redundant Converter
Error Correction Circuit
Data Shift Register
N
Digital Output
Horizontal Shift Register